

Exhibit 4B

RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940; selected revisions: 4
description:
top level BOM

revision 3.942
date: 1995/08/02 06:40:58; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

Oops typo caused dout0[7] to be short to dout1[7]

revision 3.941
date: 1995/07/31 18:50:01; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

Oops drive clk54m_ABD0P700V not clk54m_ABD0P700V when the LVS netlist

revision 3.940
date: 1995/07/30 02:47:38; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Makefile.vo: change twinvia step
Makefile.tst: remove kludge from final-report
uu/uu_control.pim: Latest placement. Note this was already in top level.
i_h_euterpe_wrap.tb: Change to single configuration file

revision 3.939
date: 1995/07/29 23:46:20; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

When wrapping the LVS netlist don't expect the vdde pin to be at the interface
of euterpe - it's a global

=====

RCS file: /s6/cvsroot/euterpe/verify/status,v
Working file: verify/status
head: 3.64
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 64; selected revisions: 8
description:

revision 3.48
date: 1995/08/02 18:49:00; author: dit00; state: Exp; lines: +21 -8

Update

revision 3.47

date: 1995/08/01 22:56:18; author: dit00; state: Exp; lines: +1 -0

Update

revision 3.46

date: 1995/08/01 17:21:20; author: lisar; state: Exp; lines: +16 -0

periodic update

revision 3.45

date: 1995/07/31 22:43:12; author: dit00; state: Exp; lines: +10 -0

Update

revision 3.44

date: 1995/07/31 16:57:35; author: dit00; state: Exp; lines: +2 -0

Periodic update

revision 3.43

date: 1995/07/31 16:16:56; author: lisar; state: Exp; lines: +338 -0

periodic update

revision 3.42

date: 1995/07/30 20:42:10; author: dit00; state: Exp; lines: +18 -0

Periodic update

revision 3.41

date: 1995/07/29 20:05:38; author: dit00; state: Exp; lines: +54 -0

Periodic update
=====

RCS file: /s6/cvsroot/euterpe/verify/random/status,v

Working file: verify/random/status

head: 2.26

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 26; selected revisions: 2

description:

revision 2.21

date: 1995/08/01 22:57:21; author: dit00; state: Exp; lines: +6 -0

Update

revision 2.20

date: 1995/07/29 20:29:47; author: dit00; state: Exp; lines: +2 -0

Periodic update
=====

RCS file: /s6/cvsroot/euterpe/verify/random/template,v

Working file: verify/random/template

head: 2.33

branch:

locks: strict

access list:

keyword substitution: kv

Exhibit 4B

Page 2 of 9

total revisions: 33; selected revisions: 3
description:

revision 2.26

date: 1995/08/02 18:50:53; author: dit00; state: Exp; lines: +14 -14
Update

revision 2.25

date: 1995/08/01 22:57:23; author: dit00; state: Exp; lines: +147 -141
Update

revision 2.24

date: 1995/07/29 20:29:45; author: dit00; state: Exp; lines: +16 -13
Periodic update

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/eu_debug_lvs.srl,v

Working file: verify/toplevel/eu_debug_lvs.srl

head: 41.1

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1; selected revisions: 1

description:

revision 41.1

date: 1995/07/31 18:47:44; author: lisar; state: Exp;
For the lvs netlist

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermtotest.S,v

Working file: verify/toplevel/hermtotest.S

head: 39.5

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 5; selected revisions: 2

description:

revision 39.5

date: 1995/08/01 18:37:40; author: jeffm; state: Exp; lines: +2 -2
Test did an extra machine check.

revision 39.4

date: 1995/07/31 17:32:24; author: jeffm; state: Exp; lines: +2 -2
Fixed pass3 to avoid nb antiuse preventing 2nd hermes op from going out - thus
causing a watchdog timeout with only one outstanding hermes request, instead
of two.

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/likedriverlog_lvs.srl,v

Working file: verify/toplevel/likedriverlog_lvs.srl

head: 41.1

branch:

locks: strict

Exhibit 4B

Page 3 of 9

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access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 41.1
date: 1995/07/31 18:47:42;  author: lisar;  state: Exp;
For the lvs netlist
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/nbleak_debug.sig,v
Working file: verify/toplevel/nbleak_debug.sig
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 41.1
date: 1995/08/03 23:36:27;  author: jeffm;  state: Exp;
Debug signals to be used to look for cause of nb shrinkage.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/rawdata_debug.srl,v
Working file: verify/toplevel/rawdata_debug.srl
head: 41.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 4
description:
-----
revision 41.5
date: 1995/08/02 18:47:23;  author: dit00;  state: Exp;  lines: +6 -6
Fixed some trace names
-----
revision 41.4
date: 1995/08/01 23:18:48;  author: jeffm;  state: Exp;  lines: +9 -0
Added signals to trace hermes clocks.
-----
revision 41.3
date: 1995/07/31 22:34:36;  author: jeffm;  state: Exp;  lines: +2 -2
Fixed a coupla signal names.
-----
revision 41.2
date: 1995/07/31 22:04:36;  author: jeffm;  state: Exp;  lines: +60 -18
Added more signals.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict

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access list:
keyword substitution: kv
total revisions: 148; selected revisions: 8
description:

revision 1.136
date: 1995/08/02 18:48:26; author: dit00; state: Exp; lines: +2 -2
Update

revision 1.135
date: 1995/07/31 23:02:30; author: lisar; state: Exp; lines: +157 -157
Add l_

revision 1.134
date: 1995/07/31 22:42:34; author: dit00; state: Exp; lines: +2 -2
More time for dram_load_config1

revision 1.133
date: 1995/07/31 22:36:16; author: lisar; state: Exp; lines: +43 -43
Add lvs list

revision 1.132
date: 1995/07/31 17:06:06; author: dit00; state: Exp; lines: +4 -4
Update

revision 1.131
date: 1995/07/30 20:42:37; author: dit00; state: Exp; lines: +3 -3
Periodic update

revision 1.130
date: 1995/07/30 00:15:58; author: lisar; state: Exp; lines: +33 -33
Add l_ simulator

revision 1.129
date: 1995/07/29 20:28:57; author: dit00; state: Exp; lines: +5 -7
Periodic update
=====

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390; selected revisions: 4
description:
top level verilog BOM

revision 4.16
date: 1995/08/02 06:40:40; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

Oops typo caused dout0[7] to be short to dout1[7]

revision 4.15

Exhibit 4B

Page 5 of 9

date: 1995/07/31 18:49:44; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

Oops drive clk54m__ABD0P700V not clk54m_AB0D0P700V when the LVS netlist

revision 4.14
date: 1995/07/30 02:47:21; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Makefile.vo: change twinvia step
Makefile.tst: remove kludge from final-report
uu/uu_control.pim: Latest placement. Note this was already in top level.
i_h_euterpe_wrap.tb: Change to single configuration file

revision 4.13
date: 1995/07/29 23:45:56; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

When wrapping the LVS netlist don't expect the vdde pin to be at the interface
of euterpe - it's a global

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737; selected revisions: 5
description:

revision 339.2
date: 1995/08/02 06:40:21; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

Oops typo caused dout0[7] to be short to dout1[7]

revision 339.1
date: 1995/07/31 18:49:25; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

Oops drive clk54m__ABD0P700V not clk54m_AB0D0P700V when the LVS netlist

revision 339.0
date: 1995/07/30 02:46:54; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Makefile.vo: change twinvia step
Makefile.tst: remove kludge from final-report
uu/uu_control.pim: Latest placement. Note this was already in top level.

i_h_euterpe_wrap.tb: Change to single configuration file

revision 338.2

date: 1995/07/30 02:46:41; author: tbr; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r

revision 338.1

date: 1995/07/29 23:45:32; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
euterpe_wrap.V

When wrapping the LVS netlist don't expect the vdde pin to be at the interface
of euterpe - it's a global
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v

Working file: verilog/bsrc/Makefile.tst

head: 40.104

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 104; selected revisions: 2

description:

revision 40.101

date: 1995/08/02 06:57:10; author: tbr; state: Exp; lines: +8 -8
make .csyn instead of .splvs to make sure we always run a check

revision 40.100

date: 1995/07/30 02:38:03; author: tbr; state: Exp; lines: +8 -9
remove kludge in final-report
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.vo,v

Working file: verilog/bsrc/Makefile.vo

head: 27.45

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 45; selected revisions: 1

description:

revision 27.43

date: 1995/07/30 02:26:38; author: tbr; state: Exp; lines: +2 -2
remove -vlh and -v2h from twinvia per wampler
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v

Working file: verilog/bsrc/euterpe.status

head: 24.83

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 83; selected revisions: 1

Exhibit 4B

Page 7 of 9

description:

revision 24.77

date: 1995/08/01 02:08:23; author: mws; state: Exp; lines: +27 -5

Add note of bug that SAAS treats its src=dst register as a pair
for source dependency analysis even though it is architecturally single octlt.
Add note of possible tricky perf improvement to skip BHicMid and get directly
to BFetch on sequentially entered ICache lines that miss.
Expand on note of CC being busy longer on ICache misses to guarantee
forward progress.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe_wrap.V,v

Working file: verilog/bsrc/euterpe_wrap.V

head: 15.104

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 104; selected revisions: 3

description:

revision 15.100

date: 1995/08/02 06:40:00; author: lisar; state: Exp; lines: +2 -2

Oops typo caused dout0[7] to be short to dout1[7]

revision 15.99

date: 1995/07/31 18:49:04; author: lisar; state: Exp; lines: +6 -1

Oops drive clk54m__ABD0P700V not clk54m__ABD0P700V when the LVS netlist

revision 15.98

date: 1995/07/29 23:44:50; author: lisar; state: Exp; lines: +2 -4

When wrapping the LVS netlist don't expect the vdde pint to be at the interface
of euterpe - it's a global

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v

Working file: verilog/bsrc/uu/BOM

head: 218.1

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 480; selected revisions: 2

description:

revision 215.0

date: 1995/07/30 02:45:48; author: tbr; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Makefile.vo: change twinvia step

Makefile.tst: remove kludge from final-report

uu/uu_control.pim: Latest placement. Note this was already in top level.

i_h_euterpe_wrap.tb: Change to single configuration file

revision 214.1

Exhibit 4B

Page 8 of 9

date: 1995/07/30 02:45:39; author: tbr; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/lvs/Makefile,v
Working file: verilog/lvs/Makefile
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8; selected revisions: 2
description:

revision 1.8
date: 1995/07/31 18:51:30; author: lisar; state: Exp; lines: +2 -4
Add missing dependancy

revision 1.7
date: 1995/07/31 00:47:38; author: lisar; state: Exp; lines: +63 -19
Emergded the behavioral cache and tag into an edif2 (form the splvs) then
successfully build a non-working mif.mm! Note used xplus5.1
=====

RCS file: /s6/cvsroot/euterpe/verilog/lvs/l_euterpe_wrap.parm,v
Working file: verilog/lvs/l_euterpe_wrap.parm
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 1.2
date: 1995/07/30 00:05:59; author: lisar; state: Exp; lines: +27 -27
Append an X to the name of the cache and tag arrays.
=====